IN THE CLAIMS:

Claims 32 and 35-37 (renumbered from claims 36-38) are proposed to be amended herein. Please note that all claims currently pending and under consideration in the referenced application are shown below. Please enter these claims as amended. This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

Claims 1-9 (Canceled)

10. (Previously presented) A method of removing oxide polymer and metal polymer from a contact opening extending through at least one dielectric layer to an exposed region of a metal-containing layer on a semiconductor substrate, the method comprising applying a solution consisting essentially of a nitric acid solution on the contact opening without substantially removing the exposed region of the metal-containing layer followed by a phosphoric acid solution dip.

11. (Previously presented) The method of claim 10, further comprising applying the nitric acid solution at a concentration of between about 50% and 100% by weight.

12. (Previously presented) The method of claim 10, further comprising applying the nitric acid solution for a time span of between about 10 seconds and 30 minutes.

13. (Previously presented) The method of claim 12, further comprising applying the nitric acid solution in a time span of about 200 seconds.

14. (Previously presented) The method of claim 10, further comprising applying the nitric acid solution at a temperature of between about 10° and 80°C.

15. (Previously presented) The method of claim 10, further comprising performing the phosphoric acid solution dip at a concentration of between about 200 volumes of water to about 1 volume of phosphoric acid and about 1 volume of water to about 1 volume of phosphoric acid.

16. (Previously presented) The method of claim 10, further comprising applying the phosphoric acid solution dip at a temperature of between about 10° and 80°C.

17. (Previously presented) The method of claim 10, further comprising applying the phosphoric acid solution dip for a time span of between about 10 seconds and 10 minutes.

18. (Previously presented) The method of claim 10, wherein the phosphoric acid solution dip further includes a fluorine-containing component.

19. (Previously presented) The method of claim 18, wherein the fluorine-containing component includes hydrofluoric acid.

20. (Previously presented) The method of claim 18, wherein the fluorine-containing component includes ammonium fluoride.

21. (Previously presented) A method of fabricating a via in a dielectric layer and an underlying barrier layer for a semiconductor device, comprising:
forming a partial via in the dielectric layer to expose at least portion of the barrier layer;
cleaning the partial via having at least a portion of the barrier layer exposed with a phosphoric acid-containing solution including a fluorine-containing component;
etching the barrier layer after the cleaning to form a full via, a bottom surface thereof defined by a surface of a metal-containing trace; and
applying a nitric acid-containing solution to the full via.

22. (Previously presented) The method of claim 21, further comprising applying the nitric acid-containing solution at a concentration of between about 50% and 100% by weight.

23. (Previously presented) The method of claim 21, further comprising applying the nitric acid-containing solution for a time span of between about 10 seconds and 30 minutes.

24. (Previously presented) The method of claim 23, further comprising applying the nitric acid-containing solution in a time span of about 200 seconds.

25. (Previously presented) The method of claim 21, further comprising applying the nitric acid-containing solution at a temperature of between about 10° and 80°C.

26. (Previously presented) The method of claim 21, further comprising cleaning the partial via with the phosphoric acid -containing solution at a concentration of between about 200 volumes of water to about 1 volume of phosphoric acid and about 1 volume of water to about 1 volume of phosphoric acid.

27. (Previously presented) The method of claim 21, further comprising cleaning the partial via with the phosphoric acid-containing solution at a temperature of between about 10° and 80°C.

28. (Previously presented) The method of claim 21, further comprising cleaning the partial via with the phosphoric acid-containing solution for a time span of between about 10 seconds and 10 minutes.

29. (Canceled)

30. (Previously presented) The method of claim 21, wherein the fluorine-containing component includes hydrofluoric acid.

31. (Previously presented) The method of claim 21, wherein the fluorine-containing component includes ammonium fluoride.

32. (Currently Amended) A method of fabricating a via in a dielectric layer and an underlying barrier layer for a semiconductor device, comprising:

forming a partial via in the dielectric layer to expose at ~~least~~ least a portion of the barrier layer;

cleaning the partial via having at least a portion of the barrier layer exposed with a phosphoric acid-containing solution;

etching the barrier layer after the cleaning to form a full via, a bottom surface thereof defined by a surface of a metal-containing trace; and

applying a nitric acid-containing solution a concentration of between about 50% and 100% by weight to the full via.

33. (Previously presented) A method of fabricating a via in a dielectric layer and a barrier layer for a semiconductor device, comprising:

removing a portion of the dielectric layer overlying the barrier layer to form a partial via exposing at least portion of the barrier layer;

cleaning the partial via with a phosphoric acid-containing solution at a concentration of between about 200 volumes of water to about 1 volume of phosphoric acid and about 1 volume of water to about 1 volume of phosphoric acid;

etching the barrier layer to expose a region of a metal-containing trace underlying the barrier layer after the cleaning to form a full via ; and

applying a nitric acid-containing solution to the full via.

34. (Previously presented) A method of fabricating a via in a dielectric layer and an underlying barrier layer for a semiconductor device, comprising:

forming a partial via in the dielectric layer to expose at least portion of the barrier layer;

cleaning the partial via with a solution comprising water and phosphoric acid at a ratio of about 20:1 by volume at a temperature of about 35°C;

etching the barrier layer after the cleaning to form a full via having a metal containing trace on a bottom surface thereof; and

applying a nitric acid-containing solution to the full via.

3536. (Currently Amended) A method of fabricating a via for a semiconductor device, the method comprising:

removing at least a portion of a dielectric material exposed through an opening in an etch ~~mask~~mask;

~~to form~~ forming an oxide polymer layer on surfaces of the opening after removing at least a portion of the dielectric layer;

removing a barrier layer underlying the opening to expose at least a portion of a metal-containing layer and to form a metal polymer layer over the surfaces of the opening;

exposing the opening to a nitric acid-containing solution; ~~to~~

substantially ~~remove~~ removing the metal polymer layer without substantially removing the exposed portion of the metal-containing layer; ~~and~~

exposing the opening to a phosphoric acid-containing solution; and

~~to~~ substantially ~~remove~~removing the oxide polymer layer.

3637. (Currently Amended) The method of claim 35, wherein the exposing the opening to the phosphoric acid-containing solution is performed before the removing the barrier layer underlying the opening.

3738. (Currently Amended) The method of claim 35, wherein the exposing the opening to the ~~a~~ nitric acid-containing solution is ~~followed~~ followed by exposing the opening to a phosphoric acid-containing solution.